ABSTRACT OF THE DISCLOSURE

In one embodiment, an anti-wafer structure includes a silicon on insulator (SOI) layer and a plurality of probe dice formed on the SOI layer. Each of the probe die may have a pad layout corresponding to a pad layout of a die on a wafer under test. A plurality of holes may extend through the SOI layer and the plurality of probe dice, with each hole corresponding to a pad on a probe die. The anti-wafer structure may be advantageously used in an advanced probe card. Techniques for fabricating an anti-wafer and an advanced probe card are also disclosed.